The specification has been amended. Claims 1 and 3-12 have been amended. Claim 2 has been canceled. Examination of the amended application respectfully is requested.

The Examiner rejected claims 1, 2, 4, 5, 7, 9 and 11 under 35 USC 103 (a) as being unpatentable over *Chen* in view of *Ishio et al.* Claims 1, 4-5 and 9 have been amended. It is submitted that amended claims 1, 2, 4, 5, 7, 9 and 11 are clearly patentable over *Chen* in view of *Ishio et al.*

Claims 1 and 4 have been amended to clarify that according to the claimed invention, integrated semiconductor chips are mounted on a nonconductive interposer substrate (which permits different electrodes thereon to be electrically isolated from each other). The interposer substrate has a through-hole through which electrodes formed on one of the chips are exposed. This permits external terminals, which are to be electrically connected to the chips, to be freely provided at any locations on a surface of the interposer substrate that is opposite to a surface on which the chips are mounted, and further permits these connections to be made with wires shorter than in the prior art. See, for example Fig. 1, in which the electrode 24 on the chip 10 to be wired with short wires 20 through the through-hole 16 to the terminals 32 on the surface of the interposer substrate 14 opposite to the surface on which the chips 10 and 12 are mounted.

In some embodiments, which support amended claims 3, 4, 6, 7, 10, 11 and 13, at least one of the chips is smaller than the size of the through-hole, so that the entire smaller chip can be located in the through-hole, as shown, for example in Figs. 6-9. Therefore, the

thickness of the obtained semiconductor chip package can be reduced as compared with the prior art.

As acknowledged by the Examiner, *Chen* shows

1. first and second semiconductor chips 22 and 21 whose reverse surfaces oppose one another,

2. a lead 241 in which a through-hole is formed at a position corresponding to an electrode 223 on the second chip 21,

3. fixing of the second chip 21 to a surface of the lead 241 at 23,

4. fixing of the first chip 22 to the reverse surface of the second chip 21, and

5. contact points for wiring 213 and 27 for the second chip, exposed at a reverse side of the lead 21.

Further, according to the Examiner, *Ishio et al.* disclose two similar semiconductor chips 1a and 1b with electrodes for wiring on their surfaces, and one of ordinary skill in the art would have found it obvious to include electrodes for wiring on the second chip of *Chen* because *Ishio et al.* discloses electrodes of its second chip and such electrodes in *Chen* would provide outside electrical connectivity.

However, such a combination would not provide the claimed invention, since the references, whether taken alone or in combination, fail to disclose of even suggest a nonconductive interposer substrate or its use as in the claimed invention. For example, *Chen* discloses only the electrically conductive electrode 241 and *Ishio et al.* disclose (see Fig. 2) only a die pad 5 disposed between two chips 1a and 1b and surrounded by leads 6. The leads 6 of *Ishio et al.* appear to correspond to the electrodes 241 of *Chen*. Neither

Chen's electrode 241 nor Ishio et al.'s die pad 5 correspond to the through-hole-containing nonconductive interposer substrate of the present claimed invention defined in independent claims 1 and 4. Claims 1 and 4 therefore are deemed to be clearly patentable over *Chen* and *Ishio et al.*, whether taken alone or in combination. The rejection of these claims and depending claims 5, 7, 9 and 11 accordingly should be withdrawn.

The Examiner also rejected claims 3, 6, 10 and 12 under 35 USC 103(a) as being unpatentable over *Chen, Ishio et al.,* and *Jeng et al.* The Examiner further rejected claims 8, 13 and 14 under 35 USC 103(a) as being unpatentable over *Chen, Ishio et al.,* and *Kitaoki et al.* Each of these rejected claims has all of the limitations of claim 1 (or 4) and additionally specifies a nonconductive interposer substrate having a through-hole and reverse side to reverse side alignment of the first and second chips, similarly to claim 2.

Both rejections rely upon *Chen* and *Ishio et al.* for the teachings discussed above. Moreover, it is noted that neither of *Jeng et al.* and *Kitaoki et al.* disclose features of the invention defined in amended claims 1 and 4, and similarly in amended claims 3 and 8, which are missing from *Chen* and *Ishio et al.*, as discussed above. That is, like *Chen* and *Ishio et al.*, neither of *Jeng et al.* nor *Kitaoki et al.* disclose the through-hole-containing nonconductive interposer substrate of the present claimed invention as defined in amended claims 1, 3, 4 and 8, or the advantages to be obtained thereby. Therefore, for reasons similar to those advanced above as to the patentability of amended claims 1, 4, 5, 7, 9 and 11, amended independent claims 3 and 8 and depending claims 6, 10 and 12-14 are deemed clearly to be patentable over *Chen*, *Ishio et al.*, *Jeng et al.* and *Kitaoki et al.* The rejections accordingly should be withdrawn.

Based on the above, it is submitted that the application is in condition for allowance and such a Notice, with allowed claims 1 and 3-14, is earnestly solicited.

A Excess Independent Claim charges of $84.00 is believed to be due. Please charge this or any other official fee due to our deposit account number 18-0002, and notify us accordingly.

Respectfully submitted,

June 20, 2002
Date

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Certification Under 37 C.F.R. §1.8 (if applicable)

I hereby certify that this Amendment is being deposited with the United States Postal Service as First Class Mail under 37 C.F.R. §1.8 on this **June 20, 2002** and addressed to the Commissioner for Patents, Washington, D.C. 20231.

Steven M. Rabin
Typed or printed name of person mailing the Amendment

Signature of person mailing the Amendment

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MARKED UP CLAIMS VERSION

1. (Amended) A semiconductor chip package comprising:

a first integrated semiconductor chip [on whose surface an electrode for wiring is formed; and] having a one side and a reverse side;

a first electrode for wiring formed on the first chip one side;

a nonconductive interposer substrate having opposite first and second surfaces, and having a through-hole extending therethrough from the first surface to the second surface;

a second integrated semiconductor chip [on whose surface an electrode for wiring is formed, and which is integrated and mounted with the first semiconductor chip,] having a one side and a reverse side, the second chip one side facing the interposer substrate first surface, the second chip being formed on the interposer substrate first surface; and

a second electrode for wiring formed on the second chip one side so as to be exposed through the interposer substrate through-hole, the second electrode to be wired through the through-hole to external terminals on the interposer substrate second surface,

[wherein] the first [semiconductor] chip [and] being formed on the second [semiconductor] chip [are integrated and mounted with respective] reverse [surfaces of the first semiconductor chip and the second semiconductor chip opposing one another] side with the first chip reverse side facing the second chip reverse side.

3. (Amended) A semiconductor chip package, [according to claim 1, further] comprising:

a first integrated semiconductor chip having a first chip size and having a one side and a reverse side;

a first electrode for wiring formed on the first chip one side;

a second integrated semiconductor chip having a second chip size and having a one side and a reverse side, the first chip being integrally mounted to the second chip with the second chip reverse side opposing the first chip reverse side;

a second electrode for wiring formed on the second chip one side;

[an] a nonconductive interposer [in which is formed] substrate having opposite first and second surfaces, and having [a through hole] the through-hole extending therethrough from the first surface to the second surface, the through-hole [which is]being larger than the[chip sizes of the] first [semiconductor chip] and [the]second [semiconductor chip sizes;

an adhesive sheet [which is a sheet-shaped adhesive material provided on a surface of] having opposite first and second surfaces, the adhesive sheet being formed of a sheet-shaped adhesive material provided on the interposer substrate at the interposer substrate first surface so as to cover the [through hole] through-hole, the adhesive sheet second surface being exposed through the through-hole from a side of the interposer substrate at the interposer substrate second surface,

wherein the [reverse surface of the] second [semiconductor] chip reverse side is fixed to [a reverse surface of] the adhesive sheet [which is exposed via the through hole at an interposer reverse surface side, and the reverse surface of the first semiconductor chip is fixed to a surface of the] second surface, and the first chip

reverse side is fixed to the adhesive sheet first surface so as to oppose the [reverse surface of the] second [semiconductor] chip reverse side at a position at which the second [semiconductor]chip is fixed, whereby [wherein] the second electrode [is] can be wired to any external terminals on the interposer substrate second surface.

4. (Amended) A semiconductor chip package, [according to claim 1, further] comprising:

a first integrated semiconductor chip having a first chip size and having a one side and a reverse side;

a first electrode for wiring formed on the first chip one side;

a second integrated semiconductor chip having a second chip size and having a one side and a reverse side, the first chip being integrally mounted to the second chip with the second chip reverse side opposing the first chip reverse side;

a second electrode for wiring formed on the second chip one side,

a nonconductive interposer substrate having opposite first and second surfaces, and having a through-hole extending therethrough from the first surface to the second surface, the [an] interposer [in which is formed a through hole which is smaller than a] substrate through-hole being smaller than [a] the first [semiconductor] chip size and larger than [a chip size of] the second [semiconductor] chip size,

wherein the first [semiconductor] chip is fixed to [to a surface of] the interposer substrate first surface at a portion of the [reverse surface of the] first

[semiconductor] chip[,] reverse [surface] side, such that the through-hole is covered[,] by the first chip, and

[the reverse surface of the second semiconductor chip] wherein the second chip reverse side is fixed to the [reverse surface of the] first [semiconductor] chip [which is exposed at a] reverse [surface] side, the first chip reverse side being exposed [at a reverse surface] through the through-hole from a side of the interposer [via the through hole] substrate at the interposer substrate second surface.

5. (Amended) A semiconductor chip package according to claim [2] 1, wherein the interposer substrate has[, at a reverse surface side thereof, a region which is] a sunken region, which is [sunken-in] sunken into the side of the interposer substrate at the interposer substrate second surface, and the through-hole is provided [at the sunken-in] through the sunken region.

6. (Amended) A semiconductor chip package according to claim 3, wherein the interposer substrate has, [at a reverse surface side thereof,] a sunken region, which is [sunken-in,] sunken into the side of the interposer substrate at the interposer substrate second surface, and the through-hole is provided [at] through the [sunken-in] sunken region.

7. (Amended) A semiconductor chip package according to claim 4, wherein the interposer substrate has[, at] a [reverse surface side thereof, a sunken-in] sunken

region, that is sunken into the side of the interposer substrate at the interposer substrate second surface, and the [through hole] through-hole is provided [at] through the [sunken-in] sunken region.

8. (Amended) A semiconductor chip package [according to claim 1], comprising:

a first integrated semiconductor chip having a first chip size and having a one side and a reverse side;

a first electrode for wiring formed on the first chip one side;

a second integrated semiconductor chip having a second chip size and having a one side and a reverse side, the first chip being integrally mounted to the second chip with the second chip reverse side opposing the first chip reverse side;

a second electrode for wiring formed on the second chip one side;

[an] a nonconductive interposer [in which] substrate having opposite first and second surfaces, and having a through-hole [is formed at a position corresponding to the electrode for wiring on the second semiconductor chip] extending therethrough from the first surface to the second surface; and

an adhesive sheet [which is a] formed of sheet-shaped adhesive material [larger than a chip size of the second semiconductor chip, and which is provided at a surface of] at the interposer substrate first surface so as to cover the through-hole, the adhesive sheet being larger than the second chip size and having a hole smaller than

the second chip size, second [semiconductor] chip size than the second chip size, [of the second semiconductor chip is formed,]

wherein the second [semiconductor] chip is fixed, at [a portion of the surface thereof, to a surface of] the second chip one side, to the interposer substrate second surface via the adhesive sheet,

wherein the first chip [the] reverse [surface of the first semiconductor chip] side is fixed to the [reverse surface of the] second [semiconductor] chip reverse side, and

[the] wherein the second chip electrode for wiring is exposed from the side of the interposer substrate at the interposer substrate [on the] second [semiconductor chip is exposed at a reverse surface side of the interposer via the small hole of the adhesive] surface through the adhesive sheet small hole and the adhesive sheet through-hole.

9. (Amended) A semiconductor chip package according to claim [2] 1, wherein the interposer substrate is formed of one of nonconductive tape and a glass epoxy material.

10. (Amended) A semiconductor chip package according to claim 3, wherein the interposer substrate is formed of one of nonconductive tape and a glass epoxy material.

11. (Amended) A semiconductor chip package according to claim 4, wherein the interposer substrate is formed of one of nonconductive tape and a glass epoxy material.

12. (Amended) A semiconductor chip package according to claim 8, wherein the interposer substrate is formed of one of a nonconductive tape and a glass epoxy material.